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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER
PHAM, HOAI V

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/769,699
Filing Date: February 02, 2004
Appellant(s): ZUNIGA-ORTIZ ET AL.

Jay M. Cantor
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 22, 2008 appealing from the Office action mailed April 6, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,709,901	Yamazaki et al.	03-2004
6,617,687	Akram et al.	09-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 27-28 and 30-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. [U.S. Pat. 6,709,901].

With respect to claim 31, Yamazaki et al. discloses (fig. 10B, cols. 10-11) a method for fabricating a semiconductor assembly comprising the step of:

providing a semiconductor chip (220) having a planar active surface including an integrated circuit, said integrated circuit having metallization patterns including at least one contact pad (221) at said planar active surface;

providing a protective overcoat (222) over said planar active surface, said protective overcoat including window exposing said at least one contact pad, said window having sidewalls;

providing an added conductive region (223 and 230) having at least one conductive layer (223) on said metallization pattern covering and conformal to said at least one contact pad, said sidewalls of said window and a portion of said protective overcoat surrounding said window, said added conductive region (230) having a planar outer surface, said outer surface of said added conductive region suitable to form metallurgical bonds without melting;

providing an assembly board (224) having at least one planar, metallurgically bondable terminal pad (225) in a distribution aligned with the distribution of said at least one contact pad (221);

aligning said added conductive region (223 and 230) and said at least one terminal pad (225) so that said at least one contact pad (225) is connected to a corresponding terminal pad (225); and

metallurgically bonding said added conductive region (223 and 230) and said at least one terminal pad (225) without melting said outer surface of said added conductive region (223 and 230) (fig. 10b).

With respect to claims 27 and 28, Yamazaki et al. discloses that wherein said step of depositing said at least one added conductive region (230) by electroless plating (col. 11, lines 8-9).

With respect to claim 30, Yamazaki et al. (fig. 10B) discloses that wherein said step of fabricating a planar outer surface of said added conductive layer comprises the step of depositing a second of at least one added conductive layer by using the method of support by islands (222) of protective overcoat.

With respect to claim 32, Yamazaki et al. discloses that where in said bonding comprises direct welding by metallic interdiffusion (col. 11, lines 5-15).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. [U.S. Pat. 6,709,901] previously applied, in view of Akram et al. [U.S. Pat. 6,617,687] previously applied.

Yamazaki et al. substantially discloses all the limitations as claimed above. Yamazaki et al. also discloses the step of depositing said at least one added conductive layer (230) by electroless plating. Yamazaki et al. does not explitcitly teach the step of depositing a second of at least one added conductive layer (230) by screen printing. However, Akram et al. discloses electroless plating, screen printing ..et. are known technique to depositing the conductive layer (66) (col. 11, lines 17-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the known technique such as screen printing as taught by, Akram et al. into the process of Yamazaki et al. to form conductive layer.

(10) Response to Argument

Claim 31

- Appellants argue that Yamazaki et al. either alone or in the combination is neither taught nor suggested the features as claimed in claim 31: providing an added conductive region on the metallization pattern covering and *conformal to said at least one of the contact pad, the sidewalls of said windows and a portion of the protective*

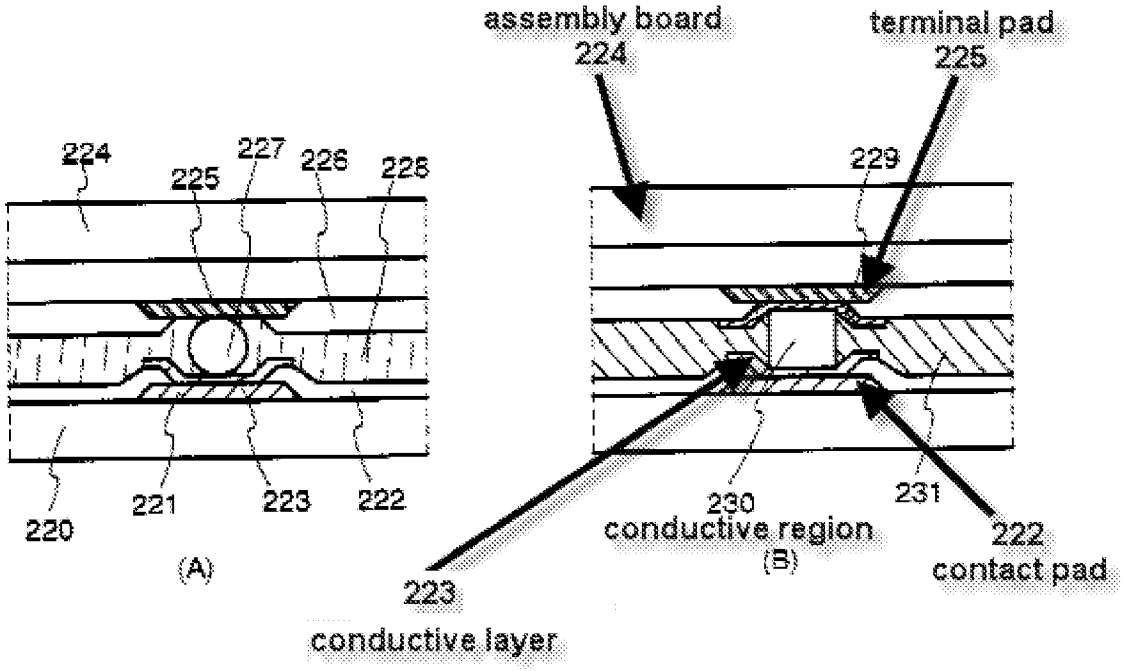
overcoat surrounding the window, the added conductive region having a planar outer surface, the outer surface of said added conductive region suitable to form metallurgical bonds without melting.

This argument is not persuasive because Yamazaki et al. (fig. 10b, col. 10, lines 46-67 and col. 11, lines 1-14) clearly disclose providing an added conductive region (223 and 230) having at least one conductive layer (223) on said metallization pattern covering and conformal to said at least one contact pad, said sidewalls of said window and a portion of said protective overcoat surrounding said window, said added conductive region (230) having a planar outer surface, said outer surface of said added conductive region suitable to form metallurgical bonds without melting.

- Appellants argue that the region 230 does not meet the requirements of claim 31 as set forth in the above paragraph since it is clearly not conformal to each of the contact pads, the sidewalls of the windows and a portion of the protective overcoat surrounding the windows, the added conductive region having a planar outer surface, the outer surface of said added conductive region suitable to form metallurgical bonds without melting.

This argument is not persuasive because the conductive layer conformal to each of the contact pads, the sidewalls of the windows and a portion of the protective overcoat surrounding the windows is the conductive layer (223) as rejected above not layer (230) as argued by Appellant. Also, the conductive region (230) having a planar outer surface, the outer surface of said added conductive region suitable to form metallurgical bonds without melting (fig. 10b, col. 11, lines 5-14).

【Fig. 10】



- Appellants further argue that no such features are taught or suggested by Yamazaki et al. either alone or in the combination as claimed in claim 31: providing an assembly board having at least one planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of the contact pads, aligning the added metallization and the board pads so that each of the contact pads is connected to a corresponding terminal pad and metallurgically bonding the chip metallization and the board pads without melting said outer surface of the added conductive region.

This argument is not persuasive because Yamazaki et al. (fig. 10b, col. 10, lines 46-67 and col. 11, lines 1-14) clearly disclose providing an assembly board (224) having at least one planar, metallurgically bondable terminal pad (225) in a distribution aligned

with the distribution of said at least one contact pad (221); aligning said added conductive region (223, 230) and said at least one terminal pad (225) so that said at least one contact pad (225) is connected to a corresponding terminal pad (221); and metallurgically bonding said added conductive region (223 and 230) and said at least one terminal pad (225) without melting said outer surface of said added conductive region (223 and 230).

Claim 27

- Appellants argue that no such combination is taught or suggested by Yamazaki et al. the limitation of depositing be selected from a group consisting of sputtering, evaporating, and plating.

This argument is not persuasive because Yamazaki et al. (col. 11, lines 8-9) clearly disclose said at least one added conductive region (230) by plating.

Claim 28

- Appellants argue that no such combination is taught or suggested by Yamazaki et al. the limitation of fabricating a planar outer surface of the added conductive region comprise the step of depositing at least one added conductive region by electroless plating.

This argument is not persuasive because Yamazaki et al. (col. 11, lines 8-9) clearly disclose that fabricating a planar outer surface of the added conductive region comprise the step of depositing at least one added conductive region (230) by electroless plating.

Claim 30

- Appellants argue that no such combination is taught or suggested by Yamazaki et al. the limitation of fabricating a planar outer surface of said added conductive layer comprises the step of depositing at least one added conductive layer by using the method of support by islands of protective overcoat.

This argument is not persuasive because Yamazaki et al. (fig. 10B) clearly disclose that wherein said step of fabricating a planar outer surface of said added conductive layer comprises the step of depositing a second of at least one added conductive layer by using the method of support by islands (222) of protective overcoat.

Claim 32

- Appellants argue that no such combination is taught or suggested by Yamazaki et al. the limitation of the bonding comprising direct welding by metallic interdiffusion.

This argument is not persuasive because Yamazaki et al. (col. 11, lines 5-15) clearly disclose that where in said bonding comprises direct welding by metallic interdiffusion.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

HP
December 10, 2008

Conferees:

Thao Xuan Le /Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

Hoai Pham /Hoai v Pham/
Primary Examiner

Darren Schuberg /Darren Schuberg/
TQAS TC 2800